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09/478,714	01/06/2000	TONY S. EL-KIK	BAYS-10-8-2	2054

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EXAMINER	
HUISMAN, DAVID J	

ART UNIT	PAPER NUMBER
2183	11

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Please find below and/or attached an Office communication concerning this application or proceeding.

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Office Action Summary	Application No. 09/478,714	Applicant(s) EL-KIK ET AL.	
	Examiner David J. Huisman	Art Unit 2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 March 2003* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-16* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-16* is/are rejected.

7)☒ Claim(s) *7* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☒ The proposed drawing correction filed on *26 March 2003* is: a)☒ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

1. Claims 1-16 have been examined.

Papers Submitted

2. It is hereby acknowledged that the following papers have been received and placed of record in the file: #8. CPA as received on 3/17/2003 and #9. Preliminary Amendment 'B' as received on 3/26/2003.

Claim Objections

3. Claim 7 is objected to because of the following informalities: The limitation claimed in lines 2-4 of claim 7 has already been claimed in parent claim 1. It is not necessary to repeat this limitation. Therefore, it is recommended that the applicant remove these lines from the claim. Appropriate correction is required.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claims 1 and 3-9 are rejected under 35 U.S.C. 102(b) as being anticipated by Campanini, U.S. Patent No. 4,700,292 (herein referred to as Campanini).

6. Referring to claim 1, Campanini has taught a dual processor system, comprising:

a) a first processor coupled to a system address bus and a data bus. See Fig.1 and note that a first processor EL_A is coupled to a bus BC, which is used to transmit both data and addresses to a second processor EL_B. For instance, during burst transfer, both a starting address is passed along BC to the second processor (making it an address bus in that it passes addresses) and the actual data to be transferred will eventually follow (making a data bus in that it passes data).

b) a second processor coupled to the system address bus and to the data bus (See Fig.1, component EL_B, the second processor comprising:

b1) a control register having a control register system address. Note the control register comprises the MEA and WCA storage locations in Fig.5. Both of these locations control the second processor during transfer mode. Also, note that these registers are read from and written to for increment and decrement purposes, respectively (see column 9, lines 27-34). Therefore, in order to read and write to specific locations, the control registers must be addressable.

b2) an internal memory. See fig.1, components DIS_B and MED_B.

b3) a data register having a data register system address and coupled to the internal memory. See Fig.4, and note the REI register. This data register receives all incoming words where the words are then propagated to the buffer store (FIFO) and ultimately, to the appropriate destination within the internal memory. Also, note that the WR signal, which indicates a write is going to occur, is used to specify a word is being transferred. See column 9, lines 27-34. Therefore, the WR signal will act as a system address for the data register in that it results in the data register receiving some data. Note also that this

data register is coupled to the internal memory since the internal memory is the final destination for the transferred words.

b4) and an internal address generator coupled to the control register and to the internal memory. See column 9, lines 26-34. Note that the MEA control register initially holds the starting internal memory address. This address is incremented by an internal address generator each time a new word is being transferred to memory.

c) a control word is written into the control register when the first processor places a control word having a burst mode bit and a starting internal address on the data bus and asserts the control register system address on the system address bus. Note that header data is sent prior to the actual data words that are to be transferred. See the abstract. This header includes the number of words to be transferred and the starting destination address. See column 2, lines 33-38, and column 8, line 61, to column 9, line 10. Note that the control register is addressed appropriately, such that the word count is put in the WCA control register and the starting address is put in the MEA register. Addresses need to be provided in order to select one of these registers.

d) the second processor enters a burst mode in which the internal address generator selects consecutive memory locations of the internal memory, starting at the starting internal address specified in the control word stored in the control register, during subsequent data transfer cycles, when the control word has a burst mode bit indicating burst mode. See column 9, lines 24-38. Note that the word count, stored in the WCA register, includes a burst mode indication. If the word count is stored as an X-bit number, then the X-1 most significant bits are the burst mode indicators. If any one of those bits is set to 1, then that bit is a burst mode bit. This can be

seen with a simple example. Suppose, one word is to be transferred (non-burst mode) and the word count is appropriately set to 00000001 (where X=8). The seven (X-1) most significant bits are set to 0, indicating that the processors are not in burst transfer mode. However, if three words were to be transferred and the word count were set to 00000011, then it can be seen that one of the seven most significant bits is set to 1, indicating burst mode. Therefore, that bit would be a burst mode bit.

e) in a write burst mode, the first processor asserts the data register system address on the system address bus and writes subsequent data words on the data bus, and the internal address generator selects consecutive memory locations of the internal memory, starting at the starting internal address, whereby the subsequent data words are written into the consecutive memory locations. See column 9, lines 24-38. Basically, the first processor asserts the WR signal, specifying a write to the data register and then transfers the data word to be written. This word will then be stored at the address specified by the MEA register, where the value of this register is incremented for as many words that are to be transferred, which is specified by the WCA register.

f) in a read burst mode, the first processor asserts the data register system address on the system address bus and reads subsequent data words on the data bus, the internal address generator selects consecutive memory locations of the internal memory, starting at the starting internal address, and the data register reads data words at the consecutive memory locations and places said data words on the data bus, whereby the subsequent data words are read from the consecutive memory locations by the first processor. See column 9, lines 24-38, and column 1, lines 7-10, and note that the relationship between processors is interchangeable, i.e., the first

processor can be the sender or the receiver. In this situation, when the first processor is to receive from the slave, this would be read mode, and it would work much like the write mode mentioned above.

7. Referring to claim 3, Campanini has taught a dual processor system as described in claim 1. Campanini has further taught that the second processor remains in the burst mode only so long as the first processor asserts the data register system address on the system address bus. From column 9, lines 24-38, as long as data is transferred to the data register (REI) via bus BC and signal WR. As long as the data register system address signal WR is applied, then data still needs to be transferred. Once there is no data left to transfer, the WR signal will not be applied, and burst mode will be finished.

8. Referring to claim 4, it has been noted by the examiner that claim 1 includes all limitations claimed in claim 4. Therefore, claim 4 is rejected for the same reasons set forth in the rejection of claim 1 above.

9. Referring to claim 5, it has been noted by the examiner that claim 1 includes all limitations claimed in claim 5. Therefore, claim 5 is rejected for the same reasons set forth in the rejection of claim 1 above.

10. Referring to claim 6, Campanini has taught a dual processor system as described in claim 1. Campanini has further taught that the second processor is a co-processor. See column 1, lines 29-43 and note that the second processor (slave) will assist the main processor if the main processor malfunctions or even if it doesn't malfunction (as described in column 3, lines 26-28).

11. Referring to claim 7, Campanini has taught a dual processor system as described in claim 1. Campanini has further taught that the second processor enters a single data transfer mode in

which the internal address generator selects the starting internal address specified in the control word stored in the control register, during a next data transfer cycle when the control word has a burst mode bit that does not indicate burst mode. As described in the rejection of claim 1(d) above, when the number of words to be transferred is 00000001 (assuming the word count register WCA holds an 8-bit value), the seven most significant bits do not indicate burst mode. Therefore, the second processor will enter a single data transfer mode, which would correspond with the value 1 in the WCA register.

12. Referring to claim 8, Campanini has taught a dual processor system as described in claim 1. Campanini has further taught that the first processor and second processor are intercoupled by

a) the system address bus and the data bus. Recall from the rejection of claim 1 that the BC bus shown in Fig.1 is a system data/address bus

b) a chip select line. See Fig.2 and note the AK signal. This signal results in the activation (selection) of the REI chip. See column 6, lines 47-55.

c) a read signal line. See Fig.2 and note the RY signal, which signifies that the second processor is ready to read transferred data. See column 6, lines 39-44.

d) a write signal line. See Fig.2 and column 9, lines 24-38 and note that the WR signal is used to signify a write operation.

13. Referring to claim 9, Campanini has taught a dual processor system as described in claim 1. Campanini has further taught:

a) the internal memory comprises a plurality of memory blocks. The internal memory has multiple addressable locations so each location can be considered a block of memory where data can be stored.

b) the control word comprises the burst mode bit field, a memory bank field which specifies a selected memory bank of the plurality of memory banks, and an internal bank address field which specifies the starting internal bank address within the selected memory bank. Again, recall the header (control word) data described in the rejection of claim 1 above. This control word contains multiple fields, where the data held in these fields is put into control registers MEA and WCA. The burst mode bit field would be the field holding the X-1 most significant bits of an X-bit word count (which is placed in the WCA register). Any one of these bits, when set, would indicate burst mode transfer. Note also that there are two banks of memory: one is referred to as the working memory, while the other is the mass memory (see Fig.1). According to the abstract, the data is first transferred to the second processor's working memory and from there it is transferred to the main memory. Therefore, the word in the MEA register can be considered both a memory bank field and an internal address bank field. This address specifies the starting memory destination address (which is incremented during burst mode). However, this word can also be interpreted as a memory bank field in that the address represents an address of the working memory, thereby implicitly selecting the working memory as opposed to selecting the mass memory.

c) the internal address generator determines the starting internal address from the selected memory bank and the internal bank address of the control word. Again, the working memory will be selected as the initial destination (not the mass memory), and the internal bank address, which is stored in the MEA register, is used as a starting address and as a subsequent address (after increment during burst transfer).

Claim Rejections - 35 USC § 103

14. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

15. Claims 2 and 10-16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Campanini, as applied above.

16. Referring to claim 2, Campanini has taught a dual processor system as described in claim 1. Campanini has not explicitly taught that the system is implemented as an integrated circuit. However, combining components to form an overall integrated circuit is well known and expected in the art. By packing everything closely together in a single circuit, higher speeds between components can be achieved and less power is dissipated. Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to implement the dual processor system as an integrated circuit.

17. Referring to claim 10, it has been noted by the examiner that the only difference between claim 1 and claim 10 is that claim 1 claims a dual processor system while claim 10 claims an integrated circuit that includes a second processor. As discussed in the rejection of claim 2 above, combining components to form an overall integrated circuit is well known and expected in the art. By packing everything closely together in a single circuit, higher speeds between components can be achieved and less power is dissipated. Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to implement the dual processor system as an integrated circuit. Consequently, claim 10 is rejected for the same

reasons set forth in the rejection of claim 1 and for the reasons above (from the rejection of claim 2).

18. Referring to claim 11, Campanini has taught an integrated circuit as described in claim 10. Furthermore, it has been noted by the examiner that the only difference between claim 3 and claim 11 is that claim 3 claims a dual processor system while claim 11 claims an integrated circuit that includes a second processor. As discussed in the rejection of claim 2 above, combining components to form an overall integrated circuit is well known and expected in the art. By packing everything closely together in a single circuit, higher speeds between components can be achieved and less power is dissipated. Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to implement the dual processor system as an integrated circuit. Consequently, claim 11 is rejected for the same reasons set forth in the rejection of claim 3 and for the reasons above (from the rejection of claim 2).

19. Referring to claim 12, it has been noted by the examiner that the only difference between claim 4 and claim 12 is that claim 4 claims a dual processor system while claim 12 claims an integrated circuit that includes a second processor. As discussed in the rejection of claim 2 above, combining components to form an overall integrated circuit is well known and expected in the art. By packing everything closely together in a single circuit, higher speeds between components can be achieved and less power is dissipated. Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to implement the dual processor system as an integrated circuit. Consequently, claim 12 is rejected for the same

reasons set forth in the rejection of claim 4 and for the reasons above (from the rejection of claim 2).

20. Referring to claim 13, it has been noted by the examiner that the only difference between claim 5 and claim 13 is that claim 5 claims a dual processor system while claim 13 claims an integrated circuit that includes a second processor. As discussed in the rejection of claim 2 above, combining components to form an overall integrated circuit is well known and expected in the art. By packing everything closely together in a single circuit, higher speeds between components can be achieved and less power is dissipated. Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to implement the dual processor system as an integrated circuit. Consequently, claim 13 is rejected for the same reasons set forth in the rejection of claim 5 and for the reasons above (from the rejection of claim 2).

21. Referring to claim 14, Campanini has taught an integrated circuit as described in claim 10. Furthermore, it has been noted by the examiner that the only difference between claim 6 and claim 14 is that claim 6 claims a dual processor system while claim 14 claims an integrated circuit that includes a second processor. As discussed in the rejection of claim 2 above, combining components to form an overall integrated circuit is well known and expected in the art. By packing everything closely together in a single circuit, higher speeds between components can be achieved and less power is dissipated. Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to implement the dual processor system as an integrated circuit. Consequently, claim 14 is rejected for the same

reasons set forth in the rejection of claim 6 and for the reasons above (from the rejection of claim 2).

22. Referring to claim 15, Campanini has taught an integrated circuit as described in claim 10. Furthermore, it has been noted by the examiner that the only difference between claim 8 and claim 15 is that claim 8 claims a dual processor system while claim 15 claims an integrated circuit that includes a second processor. As discussed in the rejection of claim 2 above, combining components to form an overall integrated circuit is well known and expected in the art. By packing everything closely together in a single circuit, higher speeds between components can be achieved and less power is dissipated. Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to implement the dual processor system as an integrated circuit. Consequently, claim 15 is rejected for the same reasons set forth in the rejection of claim 8 and for the reasons above (from the rejection of claim 2).

23. Referring to claim 16, Campanini has taught an integrated circuit as described in claim 10. Furthermore, it has been noted by the examiner that the only difference between claim 9 and claim 16 is that claim 9 claims a dual processor system while claim 16 claims an integrated circuit that includes a second processor. As discussed in the rejection of claim 2 above, combining components to form an overall integrated circuit is well known and expected in the art. By packing everything closely together in a single circuit, higher speeds between components can be achieved and less power is dissipated. Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to implement the dual processor system as an integrated circuit. Consequently, claim 16 is rejected for the same

reasons set forth in the rejection of claim 9 and for the reasons above (from the rejection of claim 2).

Conclusion

24. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Applicant is reminded that in amending in response to a rejection of claims, the patentable novelty must be clearly shown in view of the state of the art disclosed by the references cited and the objections made. Applicant must also show how the amendments avoid such references and objections. See 37 CFR § 1.111(c).

Hughes et al., U.S. Patent No. 4,481,578, has taught a direct memory access data transfer system for use with plural processors. Data is transferred from the memory of one processor to the memory of another processor without intervention by either processor.

Kawashita et al., U.S. Patent No. 4,631,671, has taught a data processing system capable of transferring single-byte and double-byte data under DMA control. A starting address and word count are also transferred to the receiving processor.

Leach et al., U.S. Patent No. 5,809,309, has taught processing devices with look-ahead instruction systems and methods. More specifically, a CPU with a DMA coprocessor has been taught where a control word is written to a control register, along with a starting address and a word count. The DMA coprocessor then proceeds to access an external memory and/or an I/O port without CPU intervention.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to David J. Huisman whose telephone number is (703) 305-7811. The examiner can normally be reached on Monday-Friday (8:00-4:30).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (703) 305-9712. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 746-7239 for regular communications and (703) 746-7238 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-3900.

DJH
David J. Huisman
May 7, 2003

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